

# **HOW TO USE DDR2 SDRAM**



# INTRODUCTION

## Readers

This manual is intended for users who design application systems using double data rate 2 synchronous DRAM (DDR2 SDRAM). Readers of this manual are required to have general knowledge in the fields of electrical engineering, logic circuits, as well as detailed knowledge of the functions and usage of conventional synchronous DRAM (SDRAM) and double data rate synchronous DRAM (DDR SDRAM).

## Legend

Caution: Information requiring particular attention

Note: Footnote for items marked with Note in the text

Remark: Supplementary information

## Related Documents

Related documents indicated in this manual may include preliminary versions, but they may not be explicitly marked as preliminary.

Document Name	Document No.
HOW TO USE SDRAM USER'S MANUAL	E0123N
HOW TO USE DDR SDRAM USER'S MANUAL	E0234E

### Notice

This document is intended to give users understanding of basic functions and usage of DDR2 SDRAM. Descriptions in this document are provided only for illustrative purpose in semiconductor product operation and application examples. And numerical values are not guaranteed values. For details about the functions of individual products, refer to the corresponding data sheet. The incorporation of these information in the design of the customer's equipment shall be done under the full responsibility of the customer. Elpida Memory, Inc. assumes no responsibility for any losses incurred by customers or third parties arising from the use of these information.

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## CHAPTER 1 ODT (ON DIE TERMINATION)

This chapter describes ODT (On Die Termination).

ODT is a new function that has been added to DDR2 SDRAM. It reduces signal reflection by including a termination resistance in the DRAM. The DRAM controller can use ODT to set the termination resistance ON and OFF simultaneously for each data I/O pin signal (DQ) as well as differential data strobe signals (DQS, /DQS, RDQS and /RDQS) and write data mask signal (DM).

By reducing signal reflection (a source of noise), this function makes for higher signal quality and thus helps enable faster data transfers.

This function also simplifies system design since it eliminates the need for layout and wiring of termination resistors. It also means there are fewer components to mount on the motherboard, which lowers part-related costs.

### 1.1 Signal Reflection

A ball that is thrown against a wall will bounce back. Similarly, electrical signals are reflected back when they reach the end of a transmission path. Electrical signals also can be reflected at points where impedance differs, such as at bus and DRAM connection points.

Signal reflection causes noise, which lowers signal quality. In a high-speed data transfer system, high-quality signals are required and even a slight amount of noise can be a major problem.

## 1.2 Motherboard Termination

Motherboard termination is a termination method that reduces signal reflection by attaching a resistor (termination resistance) with a suitable resistance value at the end of each transmission path. However, this method does not reduce signal reflection adequately in the operating frequency range used by DDR2 SDRAM. Also, adding termination resistors to the motherboard increases the component count and tends to raise costs.

### 1.2.1 Signal reflection when using motherboard termination

As mentioned above, motherboard termination may not be able to reduce signal reflection adequately. If there are several DRAMs on the same bus, such as is shown in Figure 1-1, DRAM currently being accessed is affected by reflected signals from other DRAM.

Thus, to ensure high signal quality required in a high-speed data transfer system, a processing technology is needed to control signal reflection with greater precision than is possible with motherboard termination.

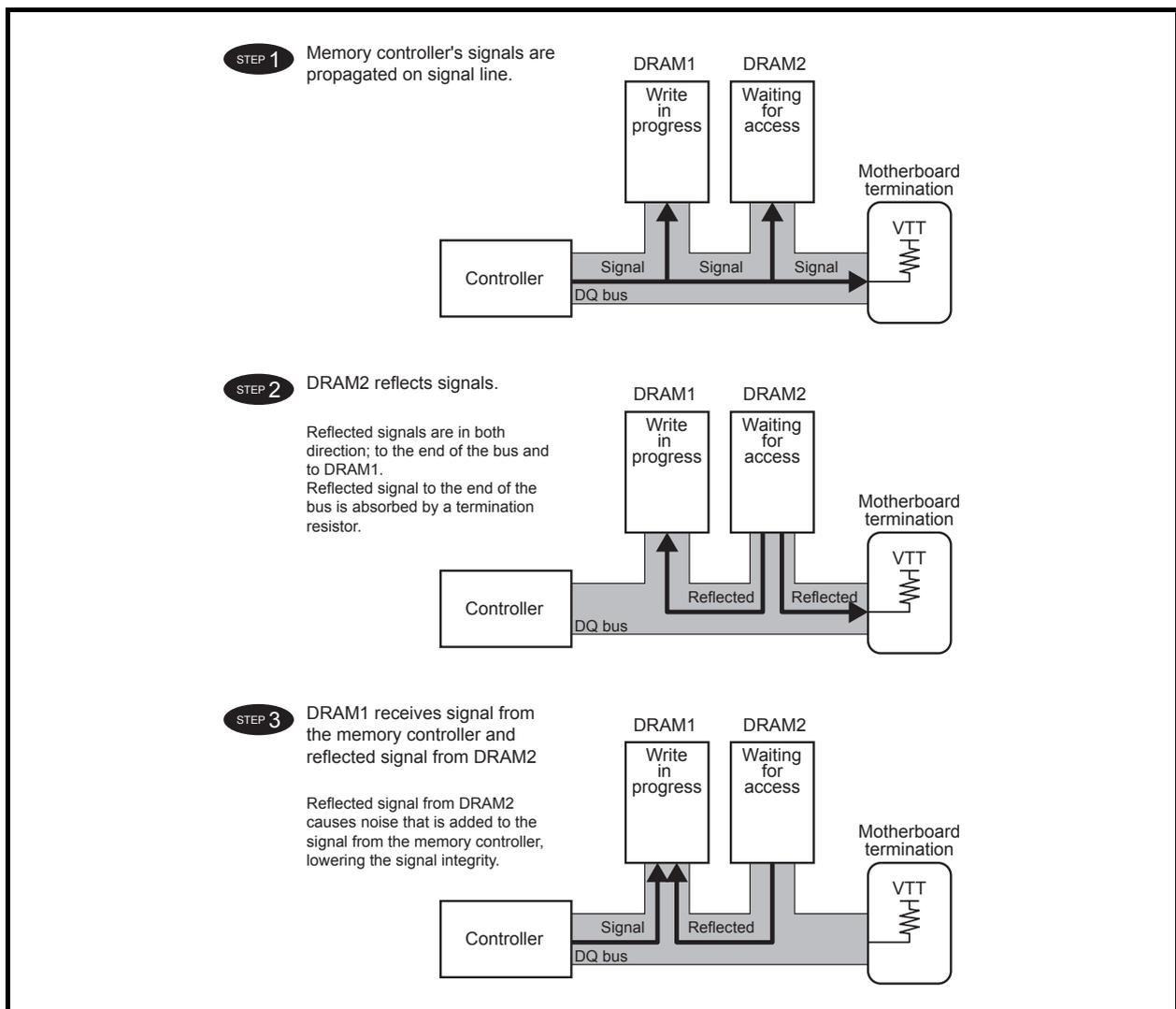


Figure 1-1 Signal Reflection when Using Motherboard Termination

### 1.3 Overview of ODT

When using ODT, the on-die termination resistance for each DRAM can be switched ON and OFF.

Accordingly, even when several DRAMs exist on the same bus, signals transmitted to the DRAM can be terminated.

As a result, DRAM currently being accessed is less likely to be affected by reflected signals from other DRAM.

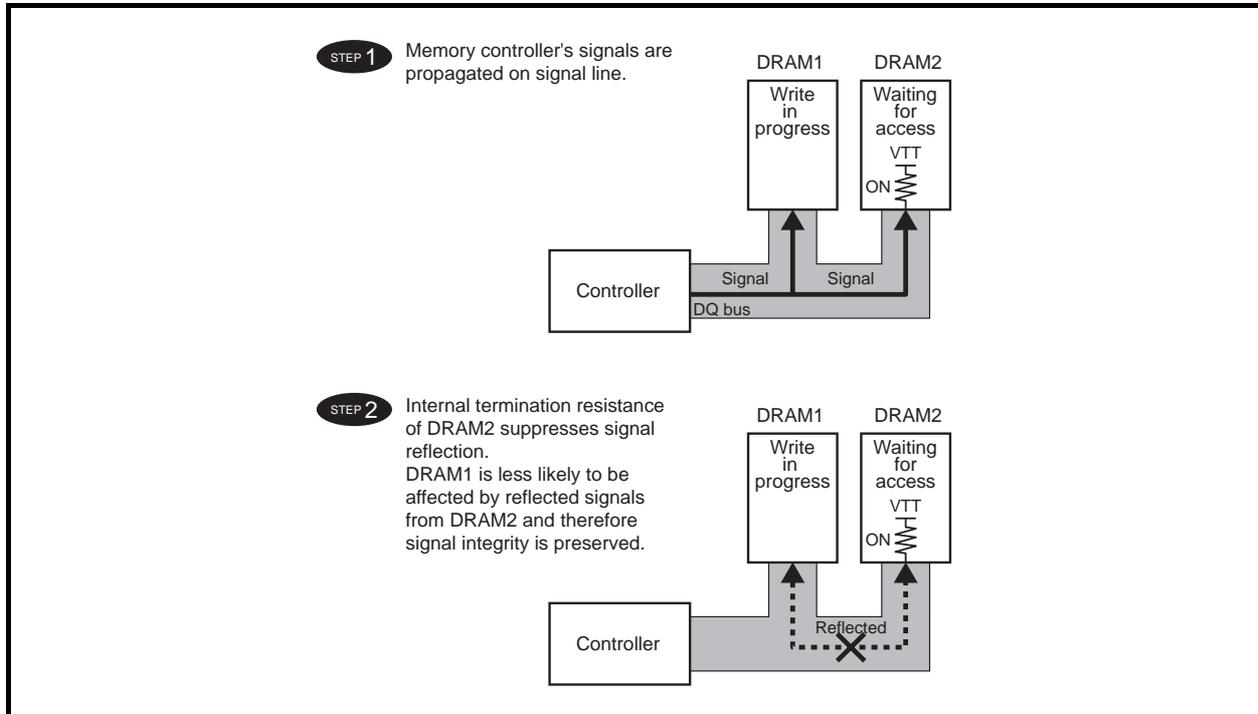


Figure 1-2 ODT and Reflected Signals

#### 1.3.1 ODT features

DDR2 SDRAM embeds the termination resistors that used to be placed on the motherboard. The DRAM controller can use ODT to set the termination resistance simultaneously to each pin (DQ, DQS, /DQS, RDQS, and /RDQS) ON and OFF.

The impedance value of the termination resistors can be selected as "ODT not selected", "ODT selected (50Ω)", "ODT selected (75Ω)", or "ODT selected (150Ω)". The value to be selected is set in advance via EMRS (1), (Extended Mode Registers Set (1)).

#### 1.3.2 Advantages of ODT

DDR2 SDRAM contains termination resistors that were previously mounted on the motherboard, thereby reducing the number of parts on the motherboard. This also eliminates some of the wiring on the motherboard, which facilitates system design.

### 1.3.3 Structure of ODT

DDR2 SDRAM can use the ODT control pin to set the termination resistance simultaneously to each pin (DQ, DQS, /DQS, RDQS, and /RDQS) ON and OFF. The termination resistor's impedance value is set in advance via EMRS (1) (Extended Mode Registers Set (1)).

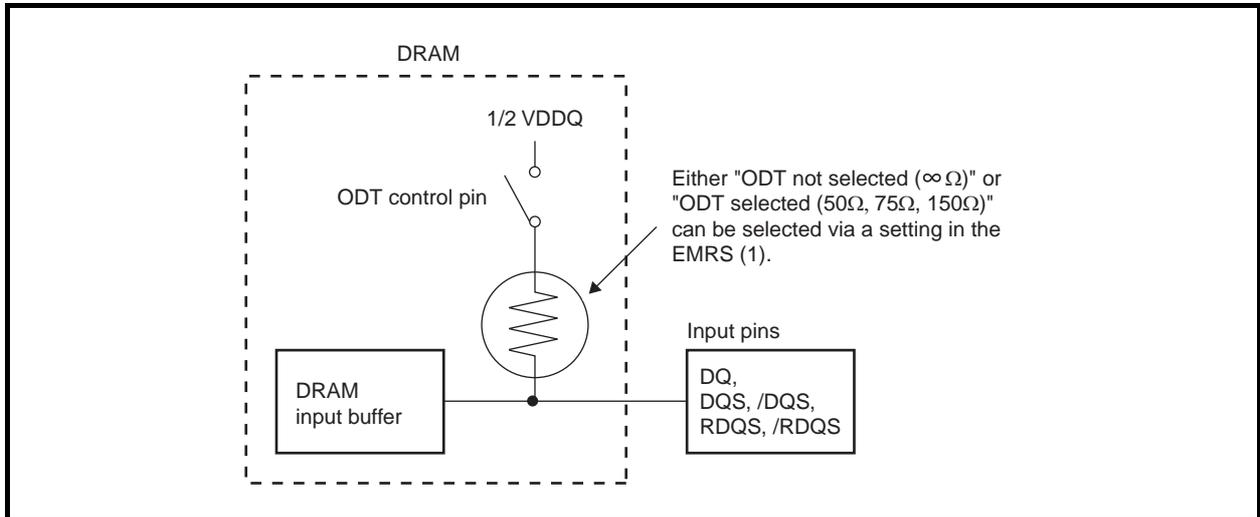


Figure 1-3 Structure of ODT

### 1.4 Setting of ODT Impedance Value

The ODT impedance value is set via EMRS (1) (Extended Mode Registers Set (1)).

Use two bits (A6 and A2) to select "ODT not selected", "ODT selected (50Ω)", "ODT selected (75Ω)", or "ODT selected (150Ω)". Once the ODT impedance value is set, the setting is retained until another setting is entered or the power is turned off.

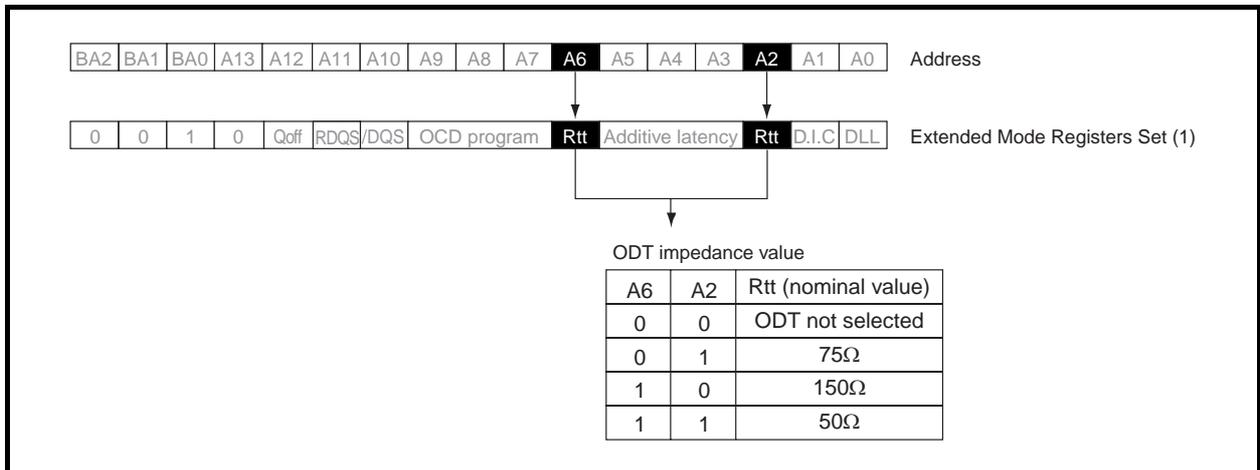


Figure 1-4 ODT Impedance Value Settings via Extended Mode Registers Set (1)

## 1.5 ODT ON/OFF Timing

The ODT settings are controlled based on the input level of the ODT control pin. The standard value of ODT timing varies between power-down mode and other modes (such as active mode or standby mode).

### 1.5.1 ODT ON/OFF timing for power-down mode

Figure 1-5 shows the ODT ON/OFF timing for power-down mode.

When ODT is set to ON (ODT control pin input is at high level) during power-down mode, the ODT turn-on delay time ( $t_{AONPD}$ ) elapses, then the internal termination resistor ( $R_{tt}$ ) is set to ON.

When ODT is set to OFF (ODT control pin input is at low level) during power-down mode, the ODT turn-off delay time ( $t_{AOFPD}$ ) elapses, then the internal termination resistor ( $R_{tt}$ ) is set to OFF.

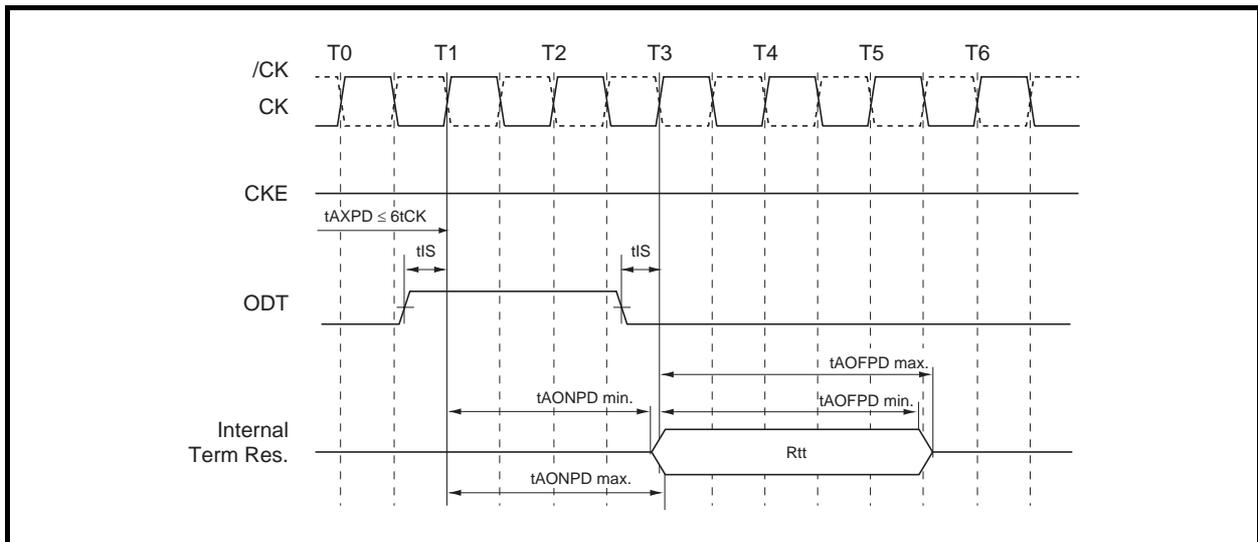


Figure 1-5 ODT ON/OFF Timing for Power-down Mode

### 1.5.2 ODT ON/OFF timing for active mode and standby mode

Figure 1-6 shows the ODT ON/OFF timing for active mode and standby mode.

When ODT is set to ON (ODT control pin input is at high level) during either standby mode or active mode, the ODT turn-on delay time ( $t_{AOND}$ ) elapses, then the internal termination resistor ( $R_{tt}$ ) is set to ON.

When ODT is set to OFF (ODT control pin input is at low level) during either standby mode or active mode, the ODT turn-off delay time ( $t_{AOFD}$ ) elapses, then the internal termination resistor ( $R_{tt}$ ) is set to OFF.

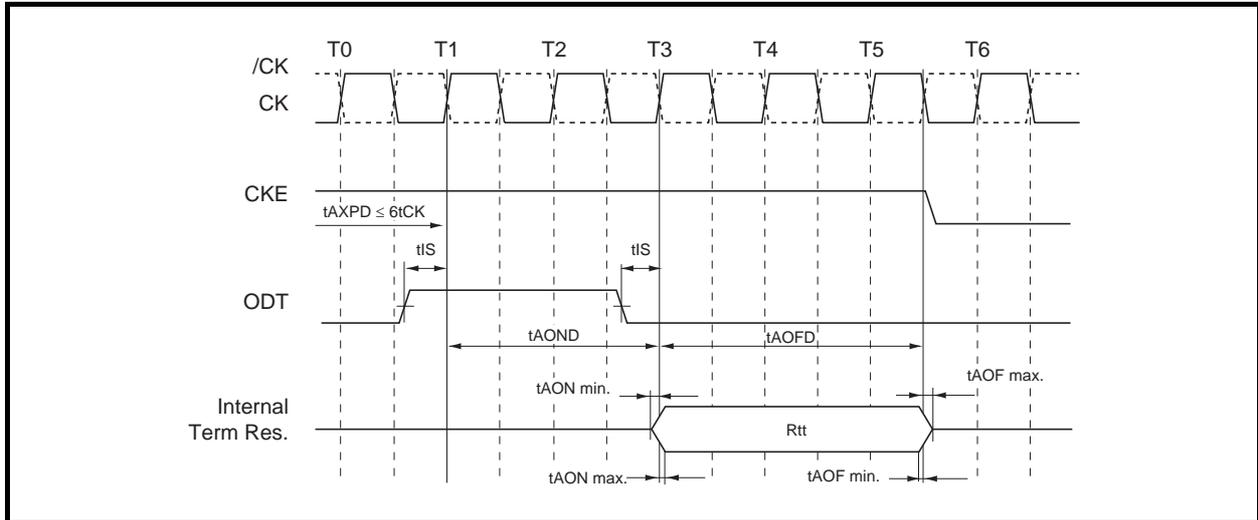


Figure 1-6 ODT ON/OFF Timing for Active Mode and Standby Mode

### 1.5.3 ODT ON timing at entering power-down mode

Figure 1-7 shows the timing when ODT is set to ON while entering power-down mode.

The turn-on delay time must elapse before ODT is turned ON. The timing differs depending on whether or not this delay time has elapsed when power-down mode is entered. If the delay time has not elapsed when power-down mode is entered, the ODT turn-on delay time will be longer than normal.

When power-down mode is entered after the ODT turn-on delay time has elapsed, DRAM is set to active mode or standby mode at the same time as power-down mode is entered.

If power-down mode is entered before ODT turn-on delay time has elapsed, the DRAM is set to power-down mode.

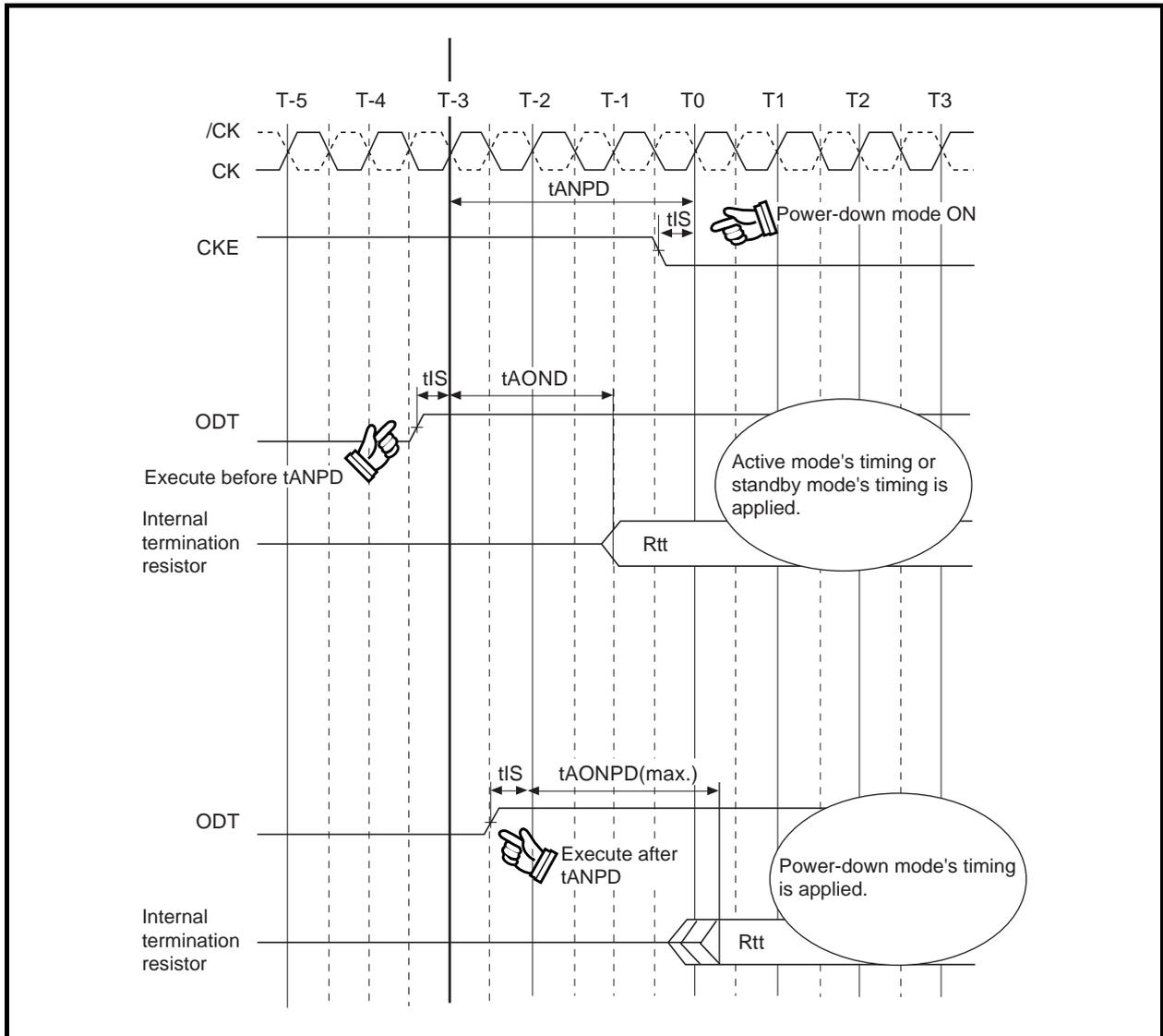


Figure 1-7 ODT ON Timing at Entering Power-down Mode

### 1.5.4 ODT OFF timing at entering power-down mode

Figure 1-8 shows the timing when ODT is set to OFF while entering power-down mode.

The turn-off delay time must elapse before ODT is turned OFF. The timing differs depending on whether or not this delay time has elapsed when power-down mode is entered. If the delay time has not elapsed when power-down mode is entered, the ODT turn-off delay time will be longer than normal.

When power-down mode is entered after the ODT turn-off delay time has elapsed, the DRAM is set to active mode or standby mode at the same time as power-down mode is entered.

If power-down mode is entered before ODT turn-off delay time has elapsed, the DRAM is set to power-down mode.

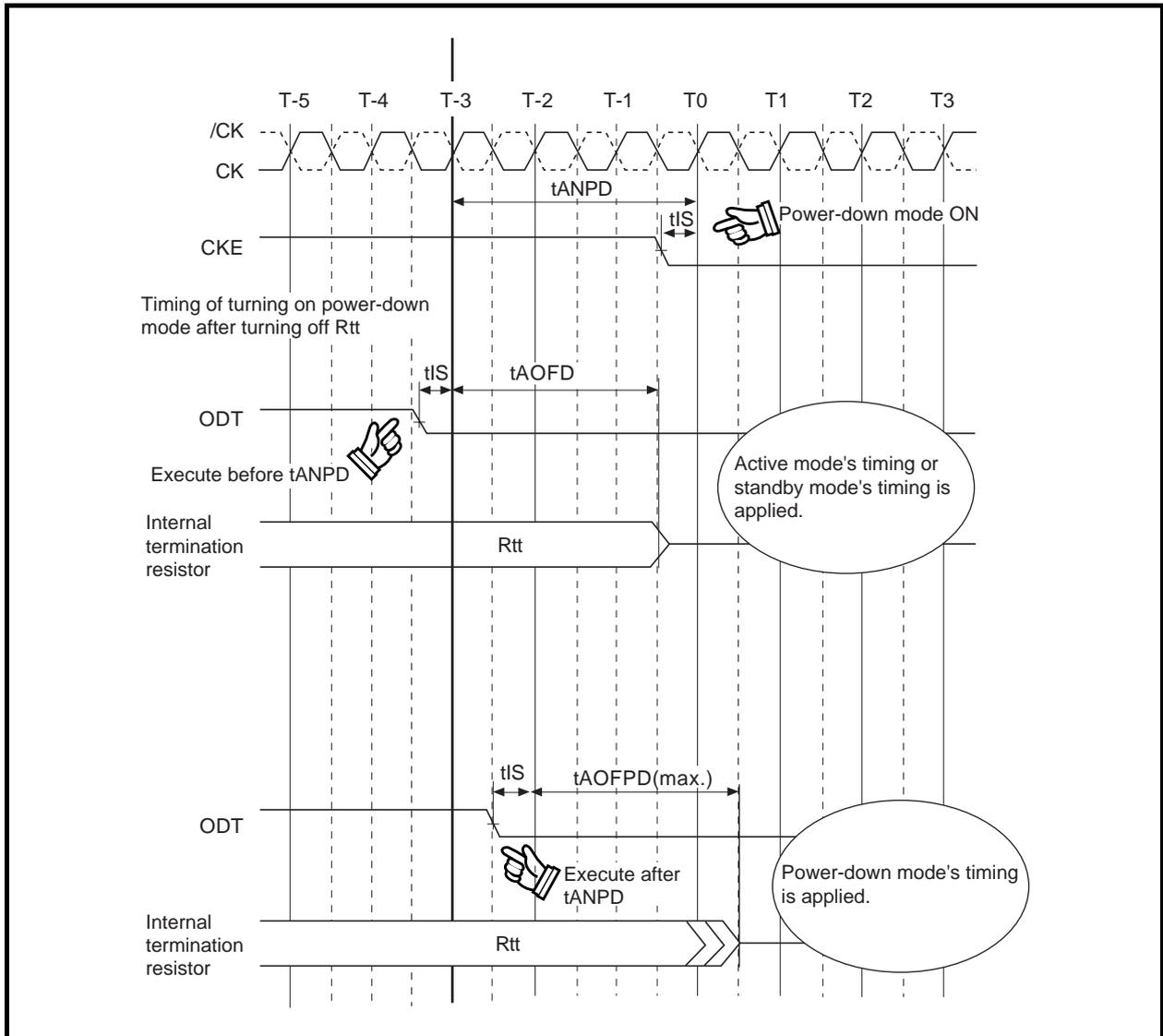


Figure 1-8 ODT OFF Timing at Entering Power-down Mode

### 1.5.5 ODT ON timing at exiting power-down mode

Figure 1-9 shows the timing when ODT is set to ON while exiting power-down mode.

The exit delay time ( $t_{AXPD}$ ) must elapse before exiting power-down mode. The timing of ODT turn-on differs depending on whether or not this delay time has elapsed.

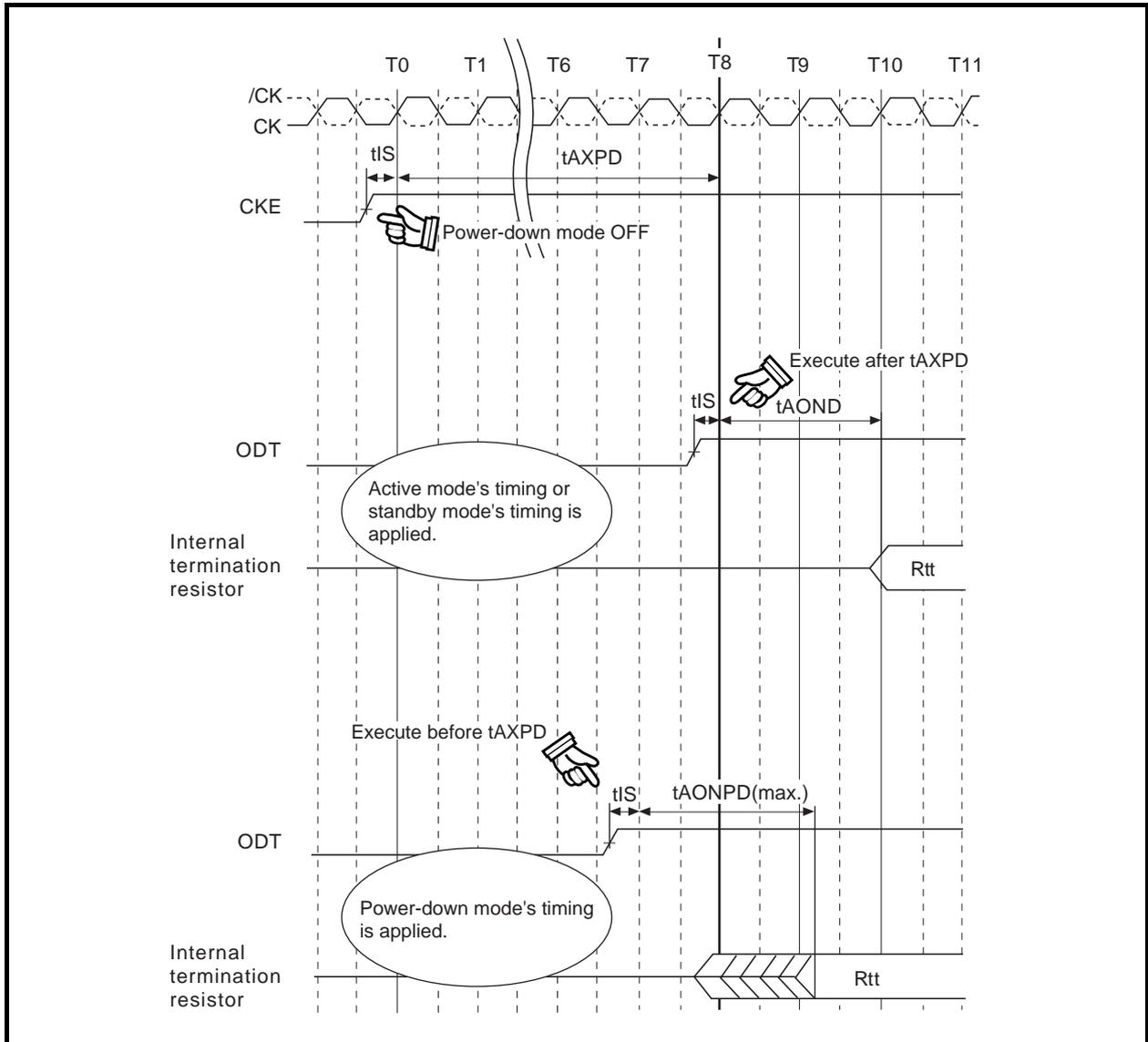
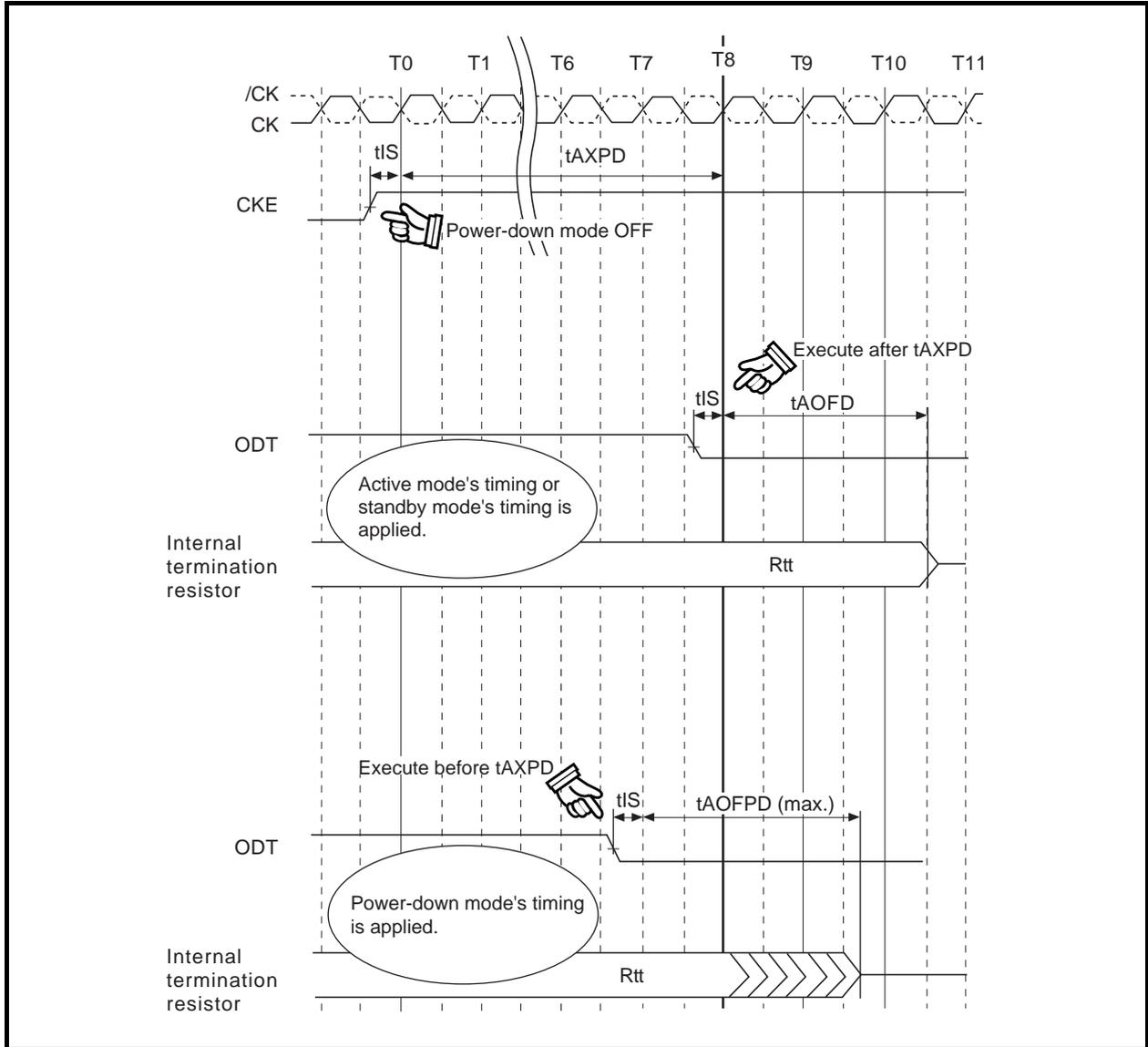


Figure 1-9 ODT ON Timing at Exiting Power-down Mode

**1.5.6 ODT OFF timing at exiting power-down mode**

Figure 1-10 shows the timing when ODT is set to OFF while exiting power-down mode.

The exit delay time ( $t_{AXPD}$ ) must elapse before exiting power-down mode. The timing for ODT turn-off differs depending on whether or not this delay time has elapsed.



**Figure 1-10 ODT OFF Timing at Exiting Power-down Mode**

**1.6 ODT in Self-refresh Mode**

ODT is not supported during self-refresh mode.

## CHAPTER 2 OCD (OFF CHIP DRIVER)

This chapter describes OCD (Off Chip Driver).

OCD is a new function that has been added to DDR2 SDRAM. It adjusts the impedance value of the DRAM's internal output driver in order to adjust the voltage so that the output signal's pull-up resistance and pull-down resistance become equal.

This function can be used to minimize unevenness in the timing of output signals. Also, when the Ron resistance fluctuates, this impedance value can be adjusted to minimize such fluctuation between devices.

OCD function is no longer necessary for DDR2 SDRAM and often used in default setting.

### 2.1 Overview of OCD

#### 2.1.1 Drive performance and transition time

When the drive performance varies, the transition time (rise time or fall time) needed for an output signal to reach any specified voltage also varies.

Figure 2-1 shows an image of how the transition times of output signals differ depending on the drive performance.

Generally, a higher drive performance means a faster signal transition time (rise time or fall time). Conversely, a lower drive performance means a slower signal transition time (rise time or fall time).

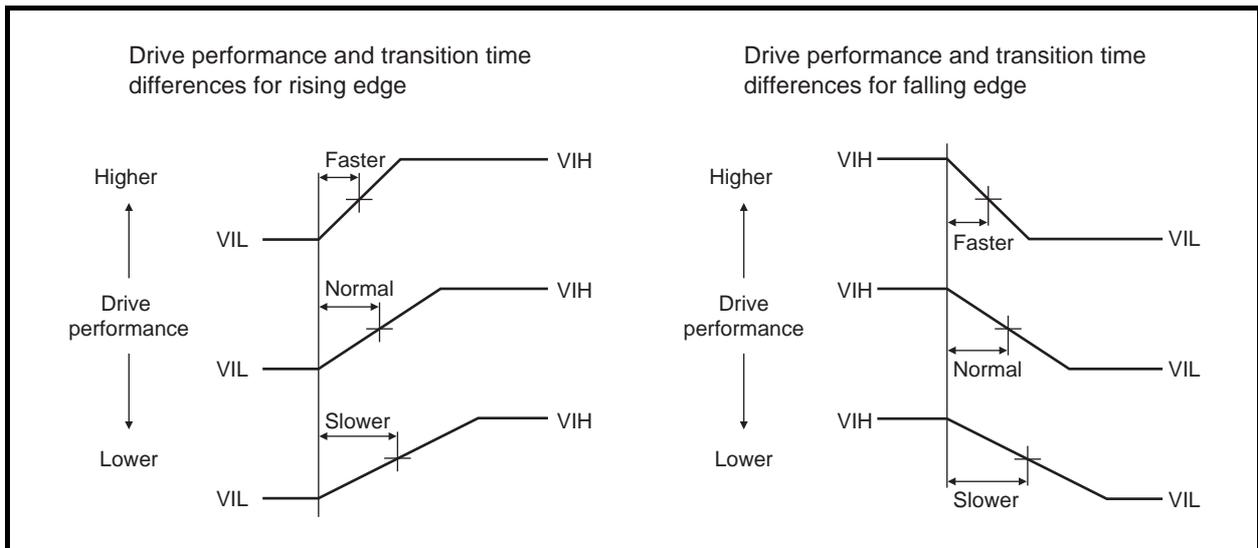


Figure 2-1 Drive Performance and Signal Transition Time

### 2.1.2 DQS signal, /DQS signal, and drive performance

The DQS and /DQS signals that are used by DDR2 SDRAM are phase related.

When the DQS and /DQS signals have the same drive performance, each signal's intermediate level and cross point also match.

However, if either signal has weaker (or stronger) drive performance than the other, the cross point and intermediate level do not match.

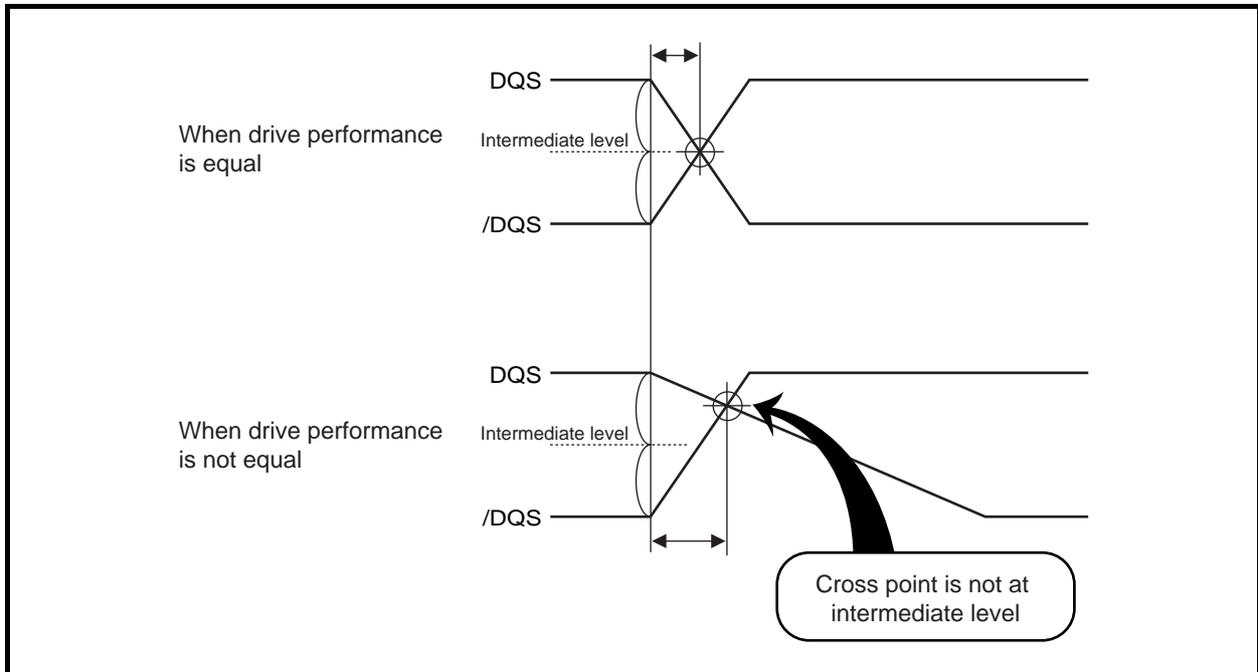


Figure 2-2 DQS Signal, /DQS Signal, and Drive performance

### 2.1.3 DQS signal, /DQS signal, and valid data window

DDR2 SDRAM uses the cross point between the DQS and /DQS signals as a reference clock for I/O data. The memory controller latches data from the DQ signal in synchronization with this reference clock. The DQ signal is referenced to distinguish the high and low levels of the VREF signal.

When the DQS and /DQS signals have different drive performances, the cross point between the DQS and /DQS signals will be offset from each signal's intermediate level. Consequently, a delay time (DQ-DQS skew) occurs between the cross point of the DQS and /DQS signals on the one hand and the cross point of the DQ and VREF signals on the other hand.

When such DQ-DQS skew exists, the time (valid data window) provided for latching data during data input or output is reduced. Reduction of this valid data window is a serious issue for DDR2 SDRAM, which require high-speed operations.

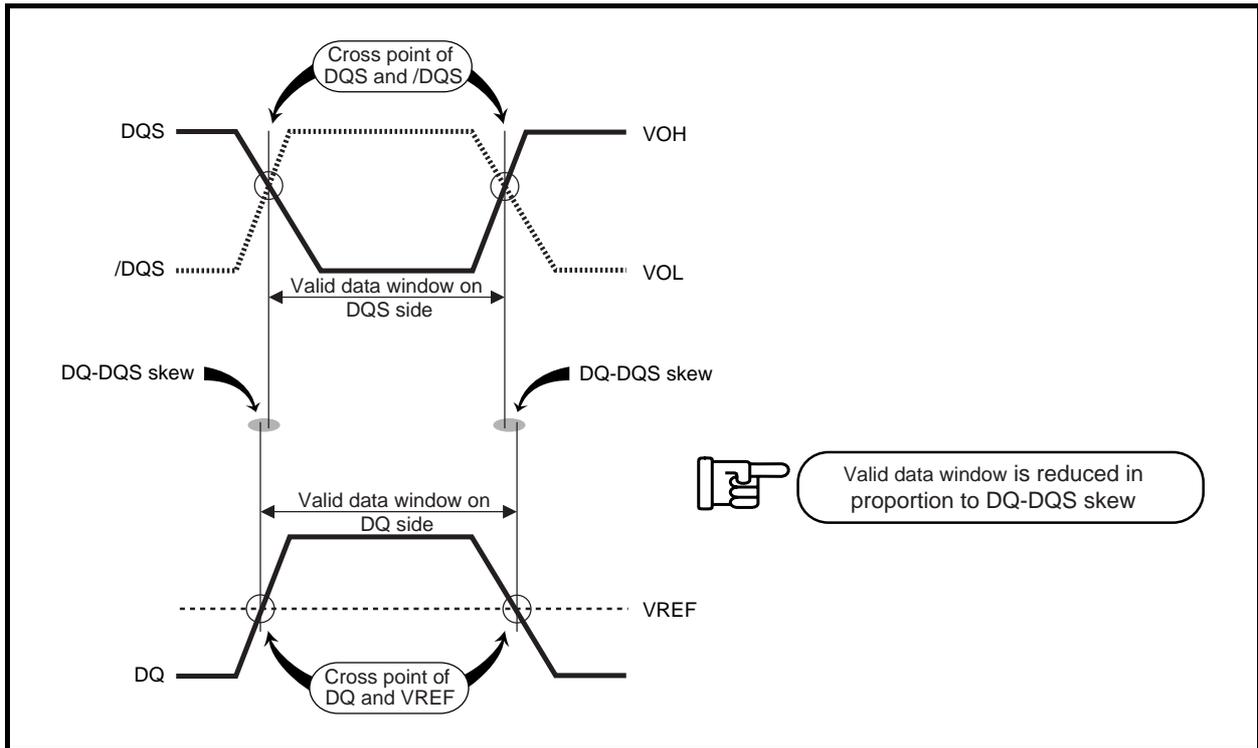


Figure 2-3 DQS Signal, /DQS Signal, and Valid Data Window

### 2.1.4 Extension of valid data window by voltage adjustment

OCD is used to adjust the impedance value of the DRAM's internal output driver. This function can adjust the voltage to equalize the pull-up resistance and pull-down resistance of the output signals (DQ, DQS, and /DQS).

When OCD is used to adjust the voltage, the cross point between the DQS and /DQS signals can be made to match the each signal's intermediate level. Optimizing the cross point between the DQS and /DQS signals minimizes the delay time for the cross point between the DQ and VREF signals.

When OCD is used to adjust the voltage with DDR2 SDRAM, DQ-DQS skew can be minimized, which maximizes the time (valid data window) provided for latching data when data is being input or output.

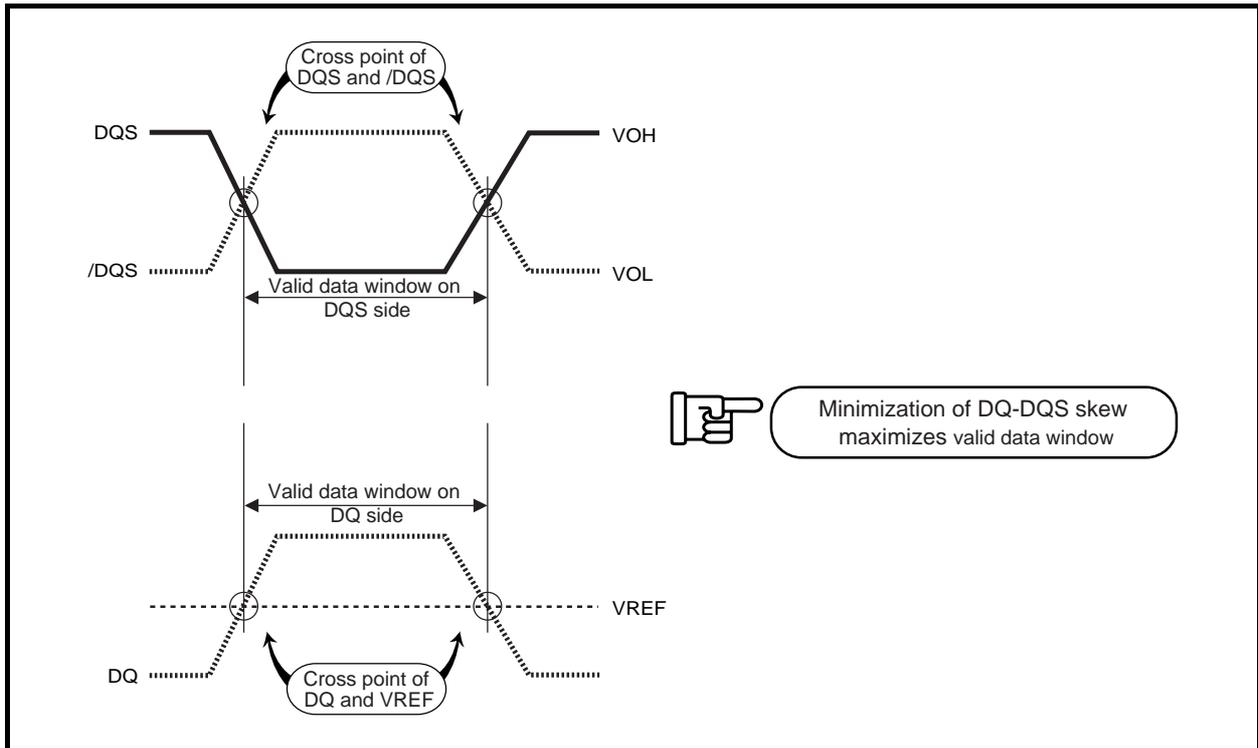


Figure 2-4 Expansion of Valid Data Window by Voltage Adjustment

## 2.2 Setting of OCD Impedance Value

The OCD impedance value is set by optimizing the impedance value of signals output by the DRAM while in drive mode, based on measurements made by the memory controller or an external measuring instrument.

During drive mode, an external device is used for comparison to determine the differential between the current impedance value and the target value (for SSTL\_18, the target value is  $18\pm 3\Omega$ ). When such a differential exists, the impedance is adjusted in adjustment mode. These comparison and adjustment steps are repeated until the optimum impedance value is set. When an OCD impedance value adjustment is being performed, all output pins are set to have the same impedance value.

### NOTE

Impedance value measurement and comparison functions are not supported by DDR2 SDRAM.

Consequently, a memory controller or other external device must be used for these measurement and comparison operations.

### 2.2.1 OCD impedance adjustment method

Five operations are performed to adjust the OCD impedance: set drive (1) mode, set drive (0) mode, set adjustment mode, OCD calibration mode exit, and set OCD calibration default. All of these operations are selected via settings in EMRS (1) (Extended Mode Registers Set (1)).

To adjust the impedance value, the pull-up resistance and pull-down resistance must be adjusted separately. This is why drive (1) mode and drive (0) mode are set.

To switch to a different mode, OCD calibration must be canceled along with the current mode.

### 2.2.2 OCD impedance adjustment steps

To adjust the impedance value, the pull-up resistance and pull-down resistance must be adjusted separately. Consequently, drive (1) mode and drive (0) mode are set. It does not matter which drive mode is set first.

Once a drive mode is set, it is determined whether or not the current impedance value is the optimum value. If the impedance value needs to be adjusted, adjustment mode is set and the impedance value is adjusted. This is repeated until the impedance value becomes the optimum value.

To switch to a different mode or to exit, OCD calibration must be canceled along with the current mode.

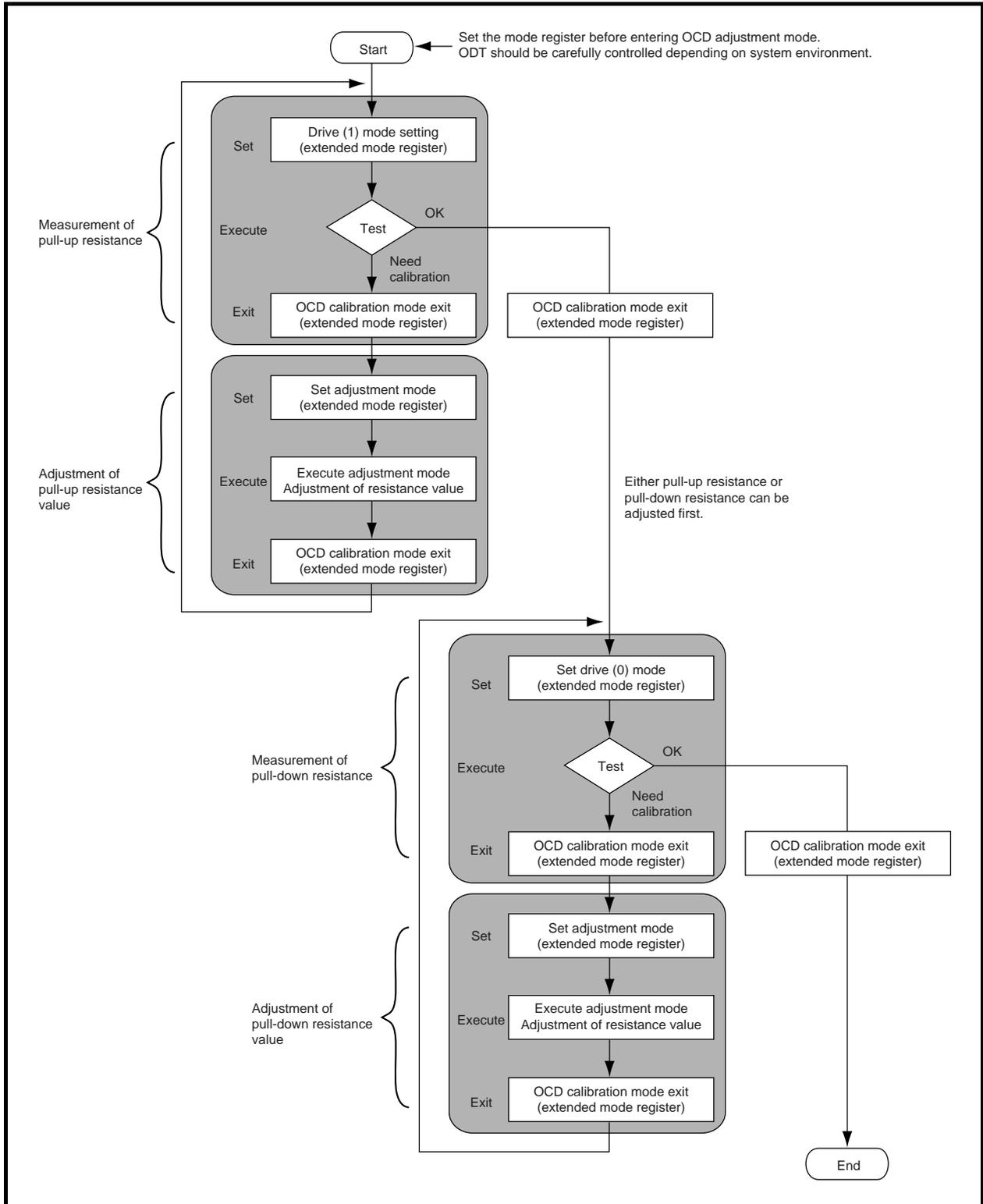


Figure 2-5 OCD Impedance Adjustment Flowchart

### 2.3 Setting of OCD Value

The OCD function's various modes are set via EMRS (1) (Extended Mode Registers Set (1)). Three bits (A7, A8, and A9) can be used to set any of five modes for OCD calibration: drive (1) mode, drive (0) mode, adjustment mode, OCD calibration mode exit, and OCD calibration default.

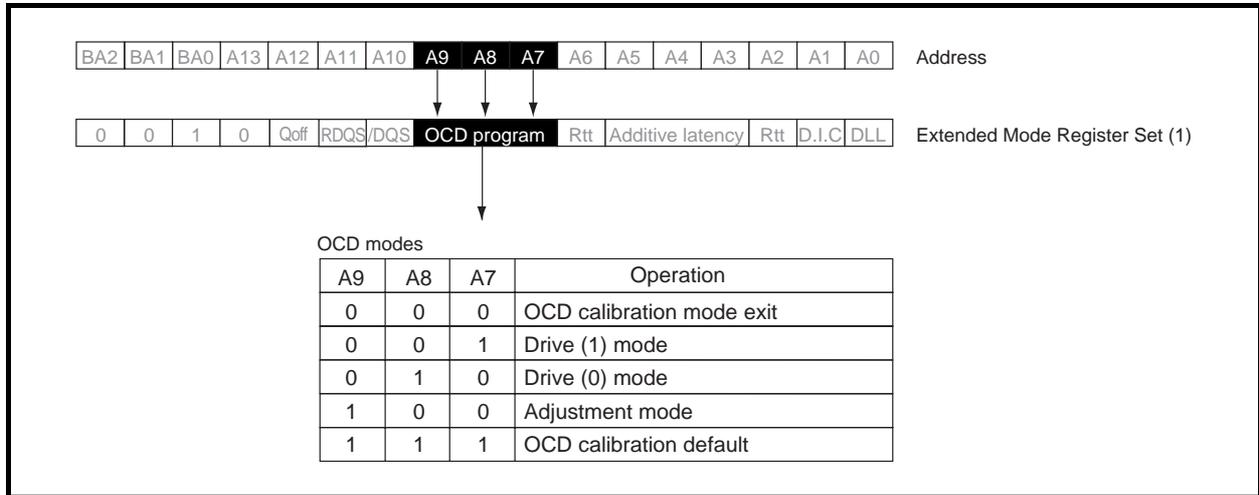


Figure 2-6 OCD Mode Settings via Extended Mode Register Set (1)

### 2.3.1 Drive (1) mode

When drive (1) mode is used, the existing status is set for the output level of output signals (DQ, DQS, and /DQS). An external device such as a memory controller must be used to measure the voltage level of the output signals (DQ, DQS, and /DQS) and determine whether or not the pull-up resistance is at the target value.

Once drive (1) mode has been set, the tOIT time must elapse before the output signals (DQ, DQS, and /DQS) are set to the output statuses listed in Table 2-1.

**Table 2-1 Output Signals When Drive (1) Mode Is Set**

Output Signal	Output Status
DQ	High level
DQS	High level
/DQS	Low level

These output statuses are maintained until the "OCD calibration mode exit" command is entered.

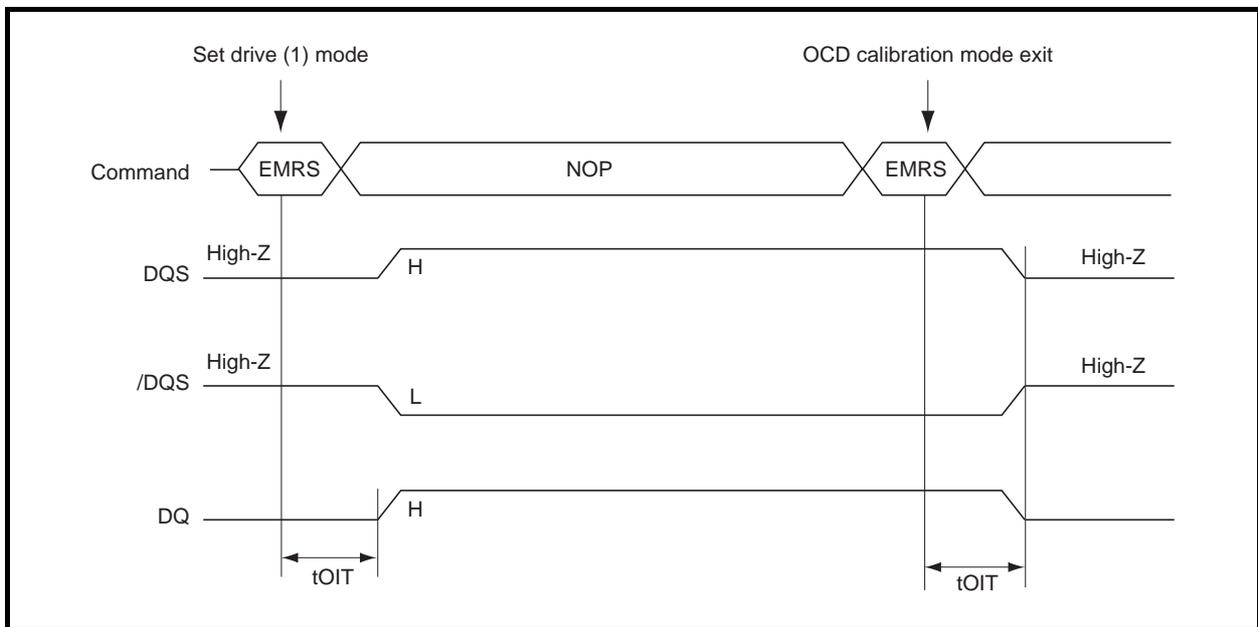
An external device is used to determine whether or not the optimum impedance value has been set for the output driver that drives the output signals (DQ, DQS, and /DQS). If this impedance value is not the optimum value, it must be reset in adjustment mode.

This cycle of measurement and adjustment is repeated until the optimum impedance value is set.

#### NOTE

Impedance value measurement and comparison functions are not supported by DDR2 SDRAM.

Consequently, a memory controller or other external device must be used for these measurement and comparison operations.



**Figure 2-7 Drive (1) Mode Timing**

### 2.3.2 Drive (0) mode

When drive (0) mode is used, the existing status is set for the output level of output signals (DQ, DQS, and /DQS). An external device such as a memory controller must be used to measure the voltage level of the output signals (DQ, DQS, and /DQS) and determine whether or not the pull-down resistance is at the target value.

Once drive (0) mode has been set, the tOIT time must elapse before the output signals (DQ, DQS, and /DQS) are set to the output statuses listed in Table 2-2.

**Table 2-2 Output Signals When Drive (0) Mode Is Set**

Output Signal	Output Status
DQ	Low level
DQS	Low level
/DQS	High level

These output statuses are maintained until the "OCD calibration mode exit" command is entered.

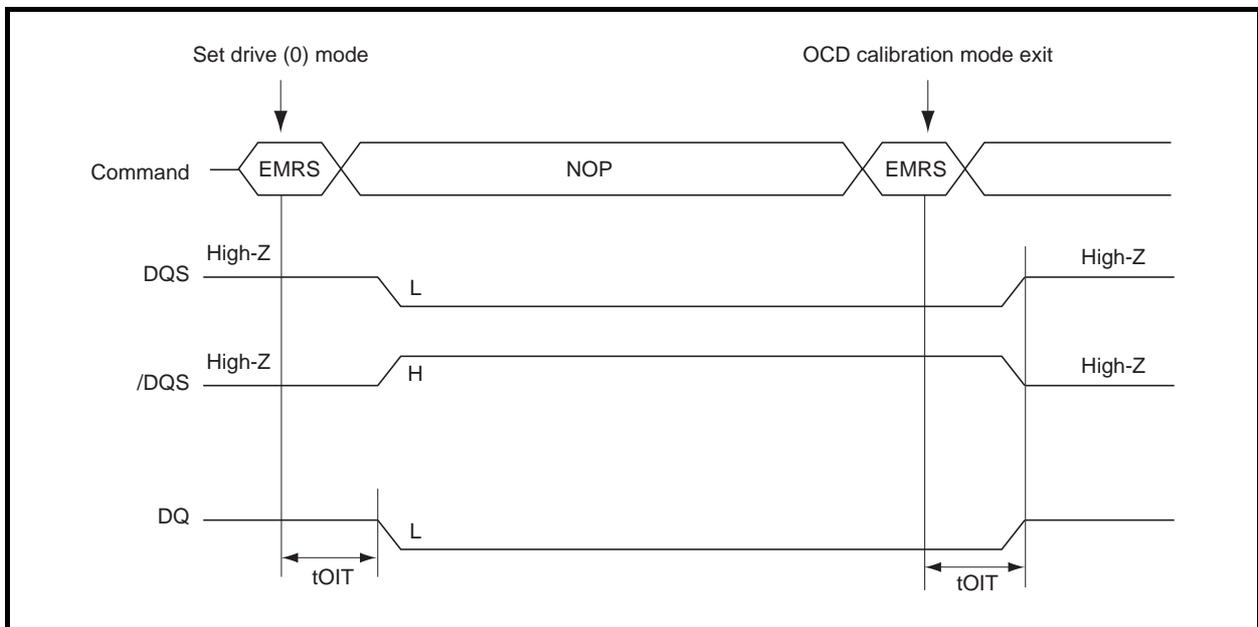
An external device is used to determine whether or not the optimum impedance value has been set for the output driver that drives the output signals (DQ, DQS, and /DQS). If this impedance value is not the optimum value, it must be reset in adjustment mode.

This cycle of measurement and adjustment is repeated until the optimum impedance value is set.

#### NOTE

Impedance value measurement and comparison functions are not supported by DDR2 SDRAM.

Consequently, a memory controller or other external device must be used for these measurement and comparison operations.



**Figure 2-8 Drive (0) Mode Timing**

### 2.3.3 Adjustment mode

Adjustment mode is used to adjust the output driver's impedance value. Since this impedance value can be adjusted among 16 levels, fine adjustment of the voltage can be performed to equalize the pull-up resistance and pull-down resistance of the output signals (DQ, DQS, and /DQS).

Once adjustment mode has been set, the write latency (WL) period must elapse, then the output driver's impedance value can be adjusted by input of four bursts of data to the DQ pin. If the output driver's impedance value has reached its limit, it cannot be adjusted upward or downward beyond that limit.

Before entering adjustment mode, the burst length must be set to "4". At that time, the input data must be input to all of the DQ pins at the same time.

Even after adjustment mode has been set, if posted CAS was used to enter commands before switching to adjustment mode, the commands are executed after the additive latency period has elapsed.

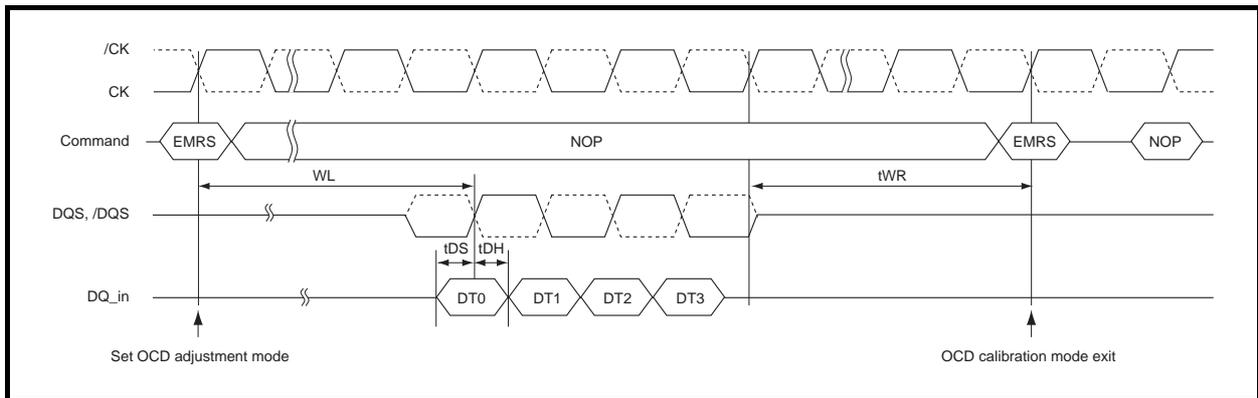


Figure 2-9 Adjustment Mode Timing

Table 2-3 Burst Data and Operations

Burst Data				Operation	
DT0	DT1	DT2	DT3	Pull-up Driver strength	Pull-down Driver strength
0	0	0	0	—	—
0	0	0	1	Increased by 1 step	—
0	0	1	0	Reduced by 1 step	—
0	1	0	0	—	Increased by 1 step
1	0	0	0	—	Reduced by 1 step
0	1	0	1	Increased by 1 step	Increased by 1 step
0	1	1	0	Reduced by 1 step	Increased by 1 step
1	0	0	1	Increased by 1 step	Reduced by 1 step
1	0	1	0	Reduced by 1 step	Reduced by 1 step
Other than above				Reserved	

**REMARKS**

1. "—" indicates no change (NOP).
2. If data other than shown above is entered, the status is the same as "—".

### 2.3.4 OCD calibration mode exit

When adjusting the OCD impedance value, the current mode must be exited before switching to another mode. The OCD calibration mode exit command is used to exit the current mode.

### 2.3.5 OCD calibration default

OCD calibration default mode sets the output driver's current impedance value to the default value. For description of the default value, see the particular product's data sheet.

### 2.3.6 Example of impedance value test circuit

The comparison circuit shown in Figure 2-10 can be used to measure impedance values. This circuit is used by an external device to determine whether or not the impedance value of the output signals (DQ, DQS, and /DQS) is at the optimum value.

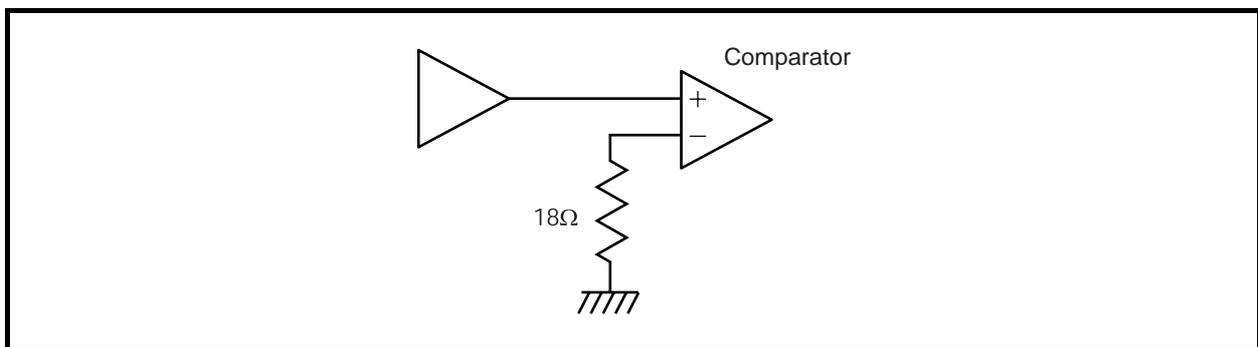


Figure 2-10 Impedance Value Test Circuit Example

## CHAPTER 3 4-BIT PREFETCH

This chapter describes the 4-bit prefetch.

The 4-bit prefetch is new architecture adopted for DDR2 SDRAM. In this architecture, the internal bus width has been made four times wider than the external bus width, so that data bus transfers can be accelerated by a factor of four without having to change the operating speed of the internal bus (memory cell array).

When using this 4-bit prefetch architecture, DDR2 SDRAM is able to perform high-speed transfers at 400Mbps or more.

### 3.1 Semiconductor Processes and Acceleration Limits

As applications become more complex, ever faster speeds are required of DRAM units. However, a DRAM unit's internal operating speed is limited under current semiconductor processes, and further acceleration is rather difficult.

Higher speed has been realized in DDR2 SDRAM by separating the DRAM's internal operations from the I/O buffer's operations to enable acceleration of the I/O buffer, which is much easier to accelerate than the DRAM itself.

### 3.2 Prefetch Operation

The prefetch operation fetches and latches in advance data that will be output from DRAM (memory cell array) to an I/O buffer.

When the operating speed of the I/O buffer is faster than that of the memory cell array, DDR SDRAM is able to increase the amount of data it can transfer in one clock cycle of a prefetch operation, which enables a data transfer area to be secured.

Two prefetch methods (4-bit prefetch and 2-bit prefetch) are provided for the prefetch operation, according to the different amounts of data that can be transferred per clock cycle. DDR2 SDRAM uses the 4-bit prefetch method.

#### 3.2.1 Operations of DDR2 SDRAM, DDR SDRAM, and SDR SDRAM

SDR SDRAM transfers data in synchronization with the rising edge of an external clock signal.

A data transfer area is secured by transferring data with  $1 \times n$  bit width (I/O width) from the memory cell array to the I/O buffer at the same frequency as the external clock signal.

DDR SDRAM transfers data in synchronization with the rising and falling edges of an external clock signal. This means that DDR SDRAM is able to transfer data at twice the speed of SDR SDRAM, even though both SDRAM types have the same operating frequency.

In addition, DDR SDRAM uses its prefetch function to latch data in  $2 \times n$ -bit width from the memory cell array to the I/O buffer at the same operating frequency as the external clock, and is thus able to secure a data transfer area without requiring a higher internal bus frequency.

DDR2 SDRAM can operate at twice the frequency of DDR SDRAM. Thus, DDR2 SDRAM is able to prefetch data in  $4 \times n$ -bit width (4-bit prefetch) without requiring a higher internal bus frequency.

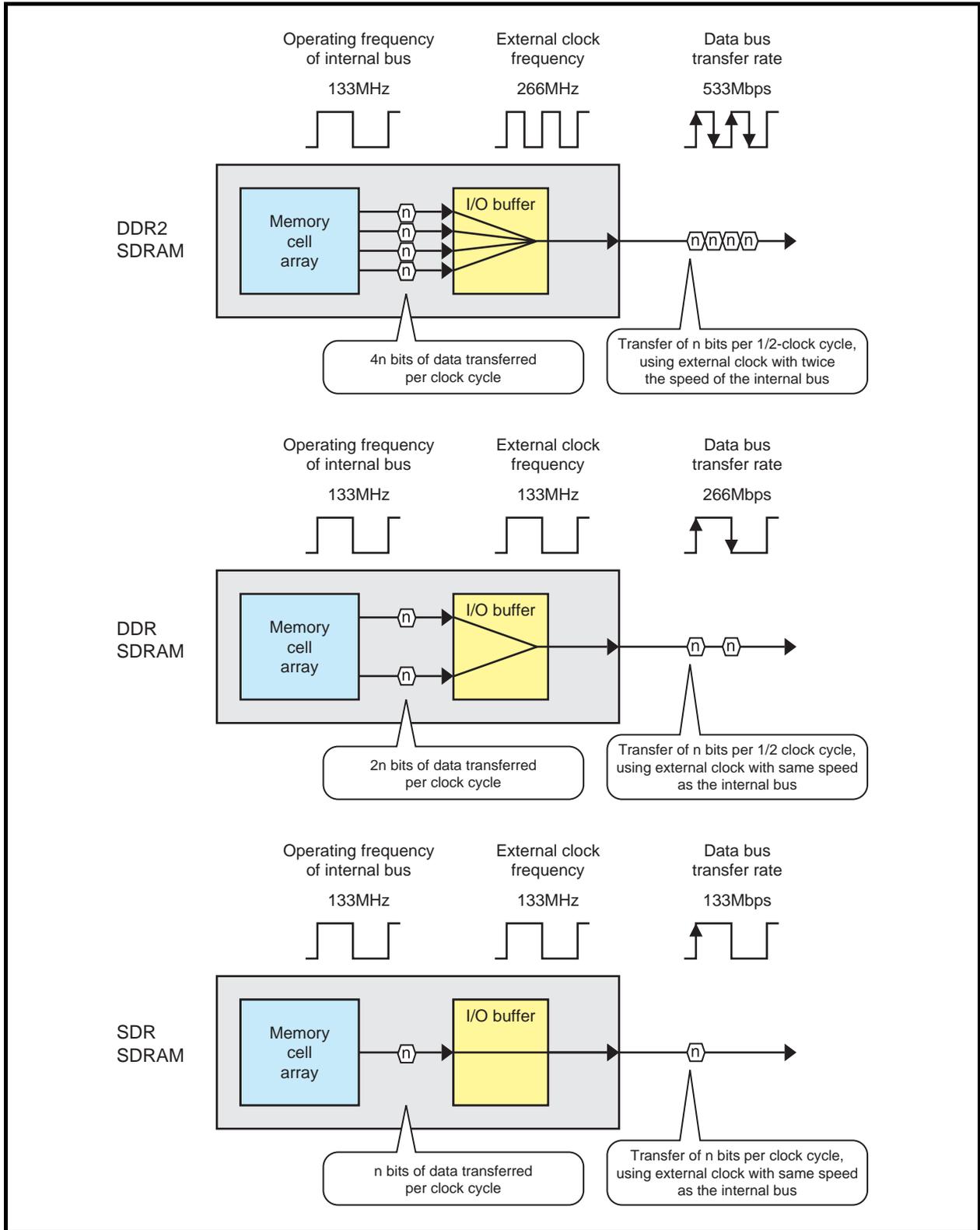


Figure 3-1 Comparison of DDR2 SDRAM, DDR SDRAM, and SDR SDRAM Operations

### 3.3 Operating Speeds of DDR2 SDRAM, DDR SDRAM, and SDR SDRAM

Table 3-1 lists the operating speeds of DDR2 SDRAM, DDR SDRAM, and SDR SDRAM when the internal bus's operating frequency is 133MHz.

A comparison of these DRAMs shows that their data bus transfer speeds vary greatly, even though they all have the same internal bus operating frequency.

In DDR SDRAM and DDR2 SDRAM, data is transferred twice as fast as in SDR SDRAM since data is transferred in at both rising and falling edges of the external clock signal. In addition, DDR2 SDRAM have twice the external clock operating frequency of DDR SDRAM, so they transfer data four times as fast as SDR SDRAM.

**Table 3-1 Operating Speeds of DDR2 SDRAM, DDR SDRAM, and SDR SDRAM**

Parameter	DDR2 SDRAM	DDR SDRAM	SDR SDRAM
Prefetch bit width	4bits	2bits	1bit
Internal bus's operating frequency	133MHz	133MHz	133MHz
External clock frequency	266MHz	133MHz	133MHz
Data bus's transfer speed	533MHz	266MHz	133MHz

## CHAPTER 4 POSTED CAS AND ADDITIVE LATENCY

This chapter describes posted CAS and additive latency (AL).

Posted CAS and additive latency are new functions that has been added to DDR2 SDRAM, which enable commands to be issued more efficiently and the effective memory area to be increased.

Posted CAS and additive latency reduce command bus conflicts to enable commands to be issued more efficiently. Consequently, more effective use of the data bus increases effective memory area of DDR2 SDRAM.

### 4.1 Overview of Posted CAS

#### 4.1.1 Problems with DDR SDRAM

When a read or write operation is performed with DDR SDRAM, first an RAS signal (for bank active command "ACT") is input, then a CAS signal (for read command "READ" or write command "WRIT") is input before the read or write operation is executed. At that time, a certain cycle interval ( $t_{RCD}$ ) is required between RAS signal input and CAS signal input. This is why command conflicts can occur when multiple read and/or write operations are executed in a series.

Even when commands are issued efficiently so as to avoid such command conflicts, wasted empty space may occur in the data bus. This reduces the efficiency of the command bus and data bus and prevents the maximum possible effective memory area from being secured.

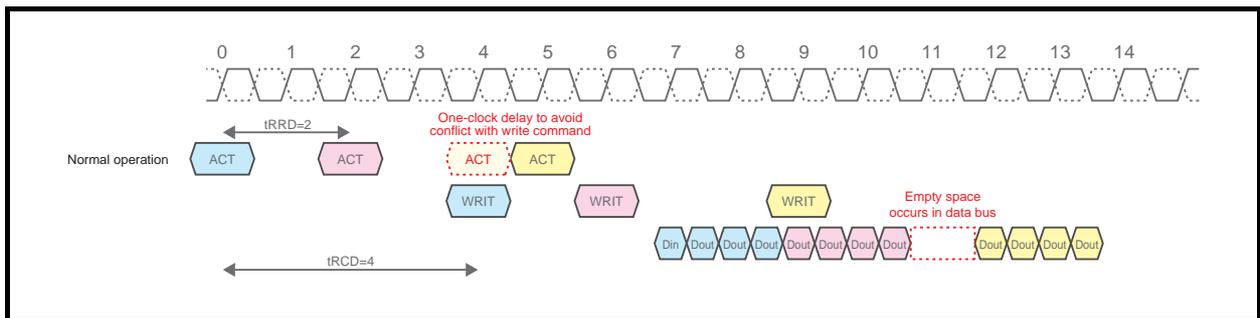


Figure 4-1 Problems with DDR SDRAM

### 4.1.2 Improvements in DDR2 SDRAM

DDR2 SDRAM use the posted CAS function to enable input of the CAS signal (for read command "READ" or write command "WRIT") either immediately after inputting the RAS signal (for bank active command "ACT") or at any time during the tRCD period. The entered read or write command is posted within the device and becomes valid after the additive latency period.

Adoption of posted CAS operations enables commands to be issued more efficiently, which also improves the efficiency of the command bus and data bus. Also, since this enables multiple read and/or writes operations to be executed consecutively, it improves the effective memory area. It also avoids command conflicts, which facilitates control via the controller.

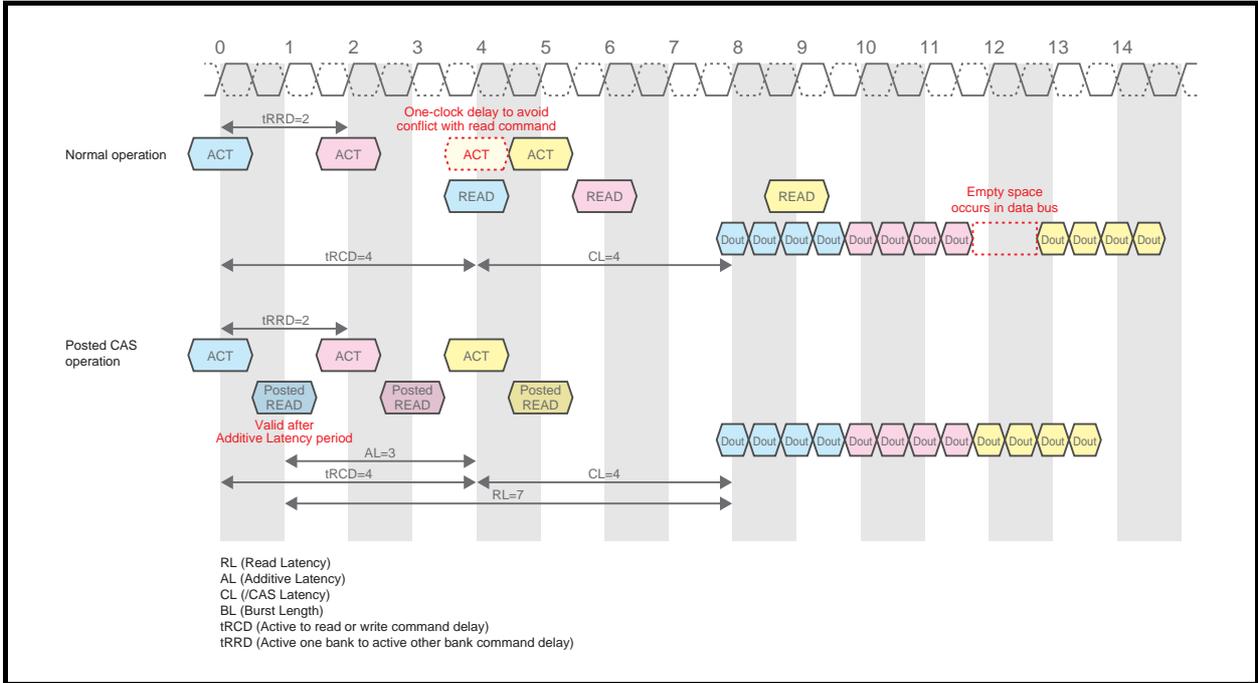


Figure 4-2 Overview of Posted CAS Operation (Read Operation)

## 4.2 Read Operation

### 4.2.1 Read operation in DDR SDRAM

Read operation in DDR SDRAM includes the following steps.

- (1) Bank active command "ACT" is input.
- (2) Read command "READ" is input after the tRCD period has elapsed following input of the bank active command.
- (3) Data output starts after the /CAS latency period "CL" has elapsed following input of the read command.

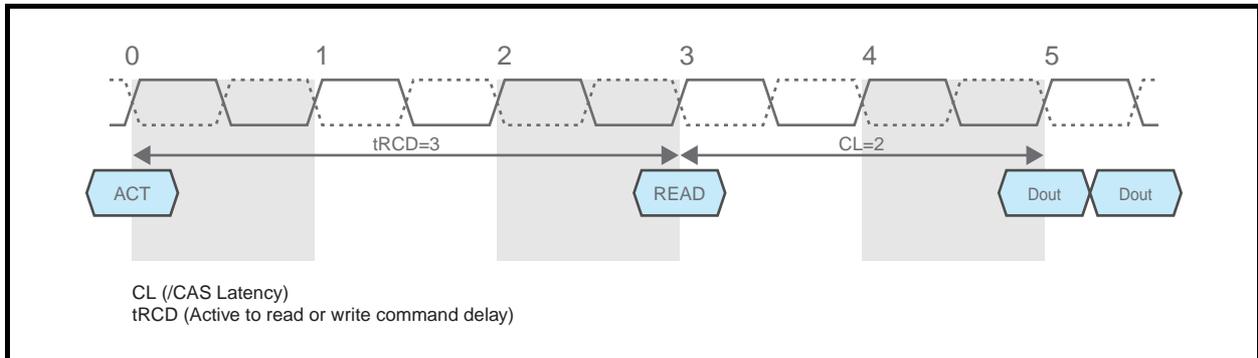


Figure 4-3 Read Operation in DDR SDRAM

When performing a series of read operations, the next bank active command can be input once the tRRD period has elapsed following input of the first bank active command, but it cannot be input via the same timing as the read command.

### 4.2.2 Read operation in DDR2 SDRAM

Read operation in DDR2 SDRAM is basically the same as that of DDR SDRAM.

- (1) Bank active command "ACT" is input.
- (2) Read command "READ" is input during the clock cycle following input of the bank active command or at any point during the tRCD period.
- (3) The read command is posted within the device and becomes valid after the additive latency (AL) period has elapsed. Data output starts after the /CAS latency period "CL" has elapsed, and after the read command became valid.

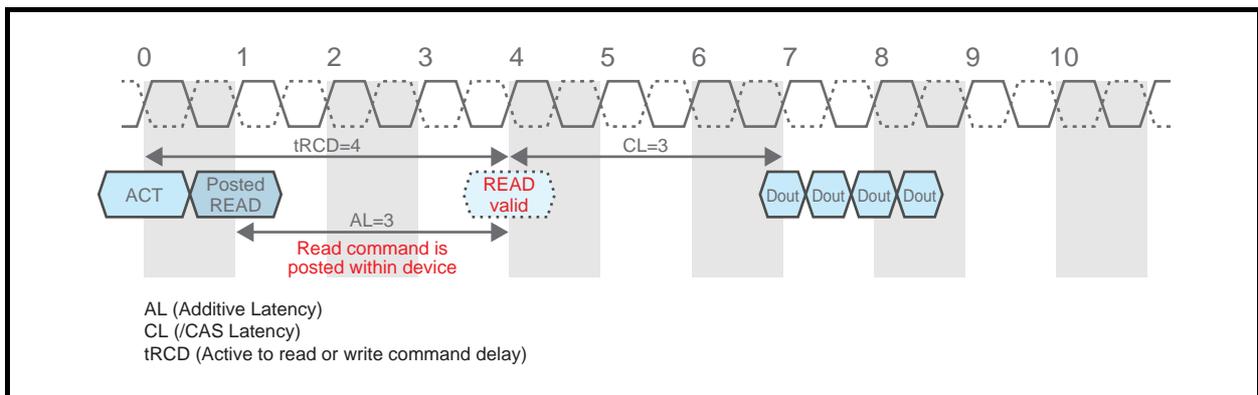


Figure 4-4 Read Operation (AL = 3) in DDR2 SDRAM

### 4.3 Write Operation

#### 4.3.1 Write operation in DDR SDRAM

Write operation in DDR SDRAM includes the following steps.

- (1) Bank active command "ACT" is input.
- (2) Write command "WRIT" is input after the tRCD period has elapsed following input of the bank active command.
- (3) Data input starts at the first rising edge of the data strobe signal following input of the write command.

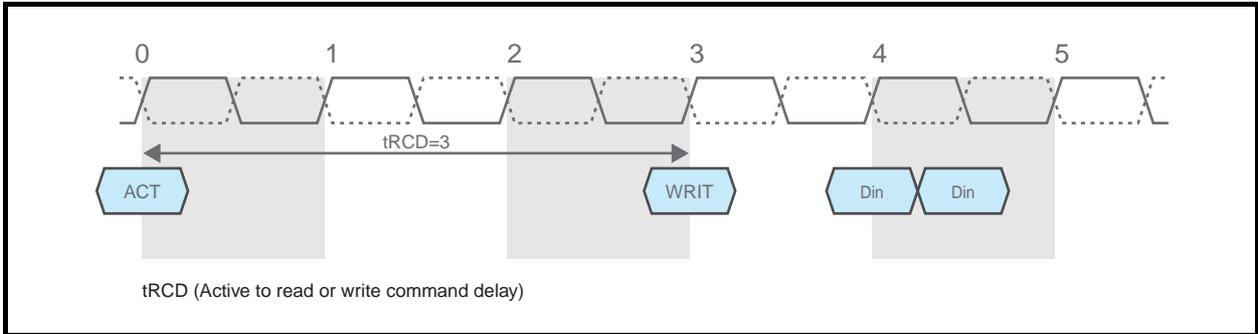


Figure 4-5 Write Operation in DDR SDRAM

When performing a series of read operations, the next bank active command can be input once the tRRD period has elapsed following input of the first bank active command, but it cannot be input via the same timing as the write command.

#### 4.3.2 Write operation in DDR2 SDRAM

Write operation in DDR2 SDRAM is basically the same as that of DDR SDRAM.

- (1) Bank active command "ACT" is input.
- (2) Write command "WRIT" is input during the clock cycle following input of the bank active command or at any point during the tRCD period.
- (3) The write command is posted within the device and becomes valid after the additive latency (AL) period has elapsed. Data input starts at the rising edge of the first data strobe signal after the write command became valid.

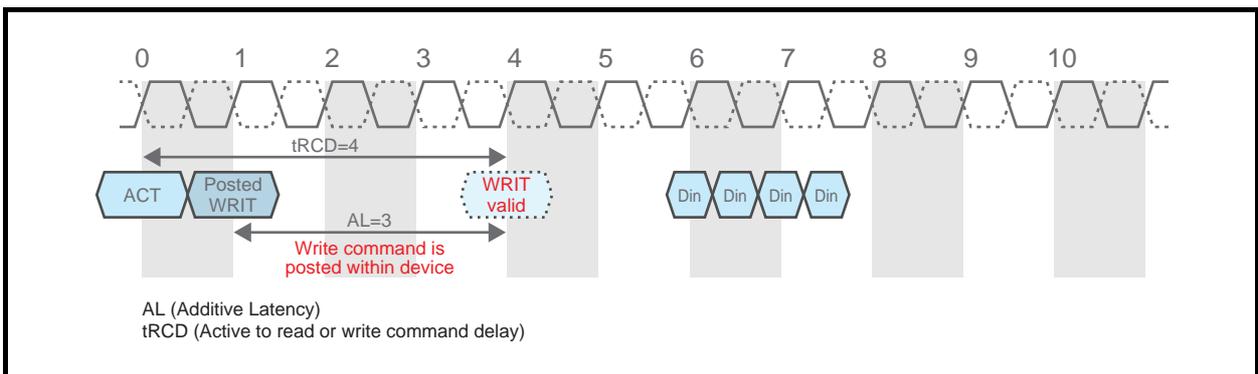


Figure 4-6 Write Operation (AL = 3) in DDR2 SDRAM

### 4.4 Setting of Additive Latency

The Additive Latency (AL) value is set via EMRS (1) (Extended Mode Registers Set (1)).

Three bits (A5 to A3) can be used to set any of five AL settings: AL = 0, AL = 1, AL = 2, AL = 3, or AL = 4.

Once the additive latency value is set, the setting is retained until another setting is entered or the power is turned off.

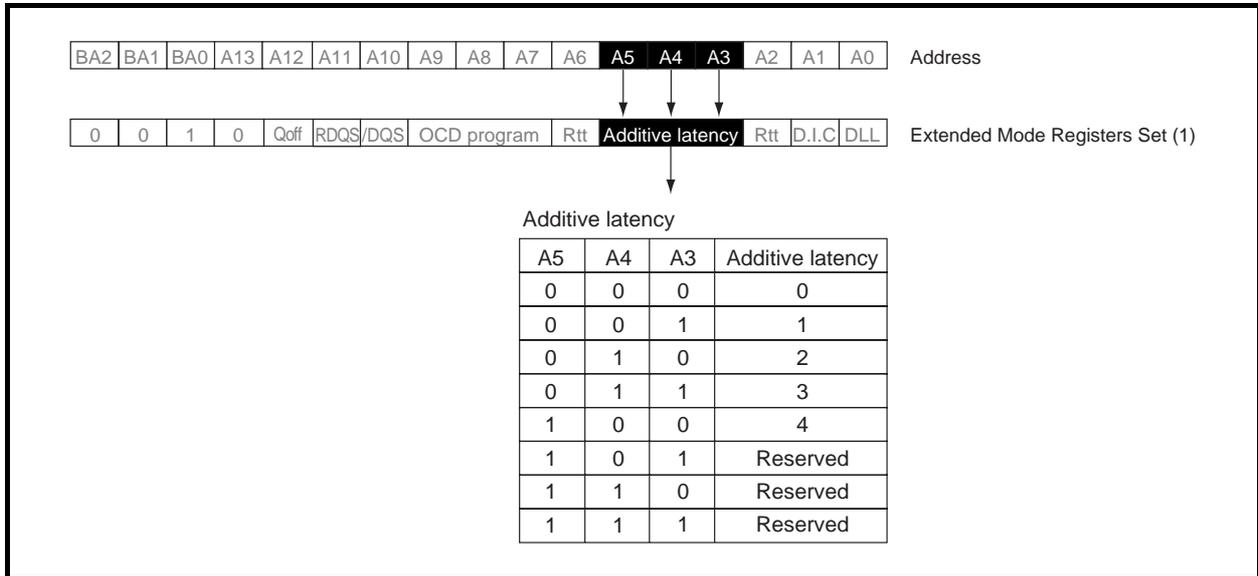


Figure 4-7 Additive Latency Setting via EMRS (1)

## 4.5 Read Latency and Write Latency

### 4.5.1 Read latency

In DDR2 SDRAM, read latency (RL) is defined as the sum of the additive latency (AL) and the CAS latency (CL) (i.e.,  $RL = AL + CL$ ).

When the additive latency value is 0 ( $AL = 0$ ), the read latency is the same as in DDR SDRAM.

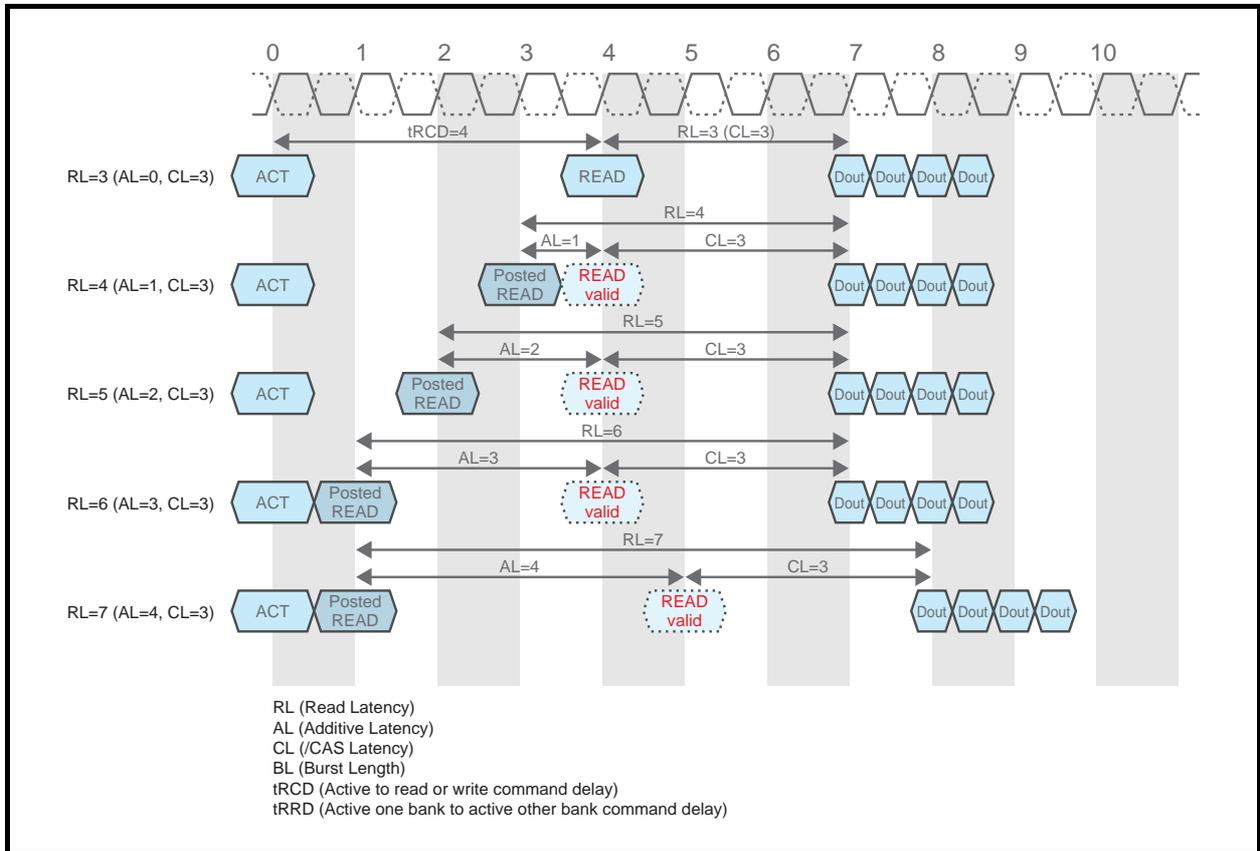


Figure 4-8 Read Latency in DDR2 SDRAM

### 4.5.2 Write latency

In DDR2 SDRAM, write latency (WL) is defined as one less than the read latency (RL) (i.e.,  $WL = RL - 1$ ). The minimum write latency is one clock cycle longer than when  $WL = 1$  in DDR SDRAM, which means  $WL = 2$  (when  $AL = 0$  and  $tRCD = 3$ ).

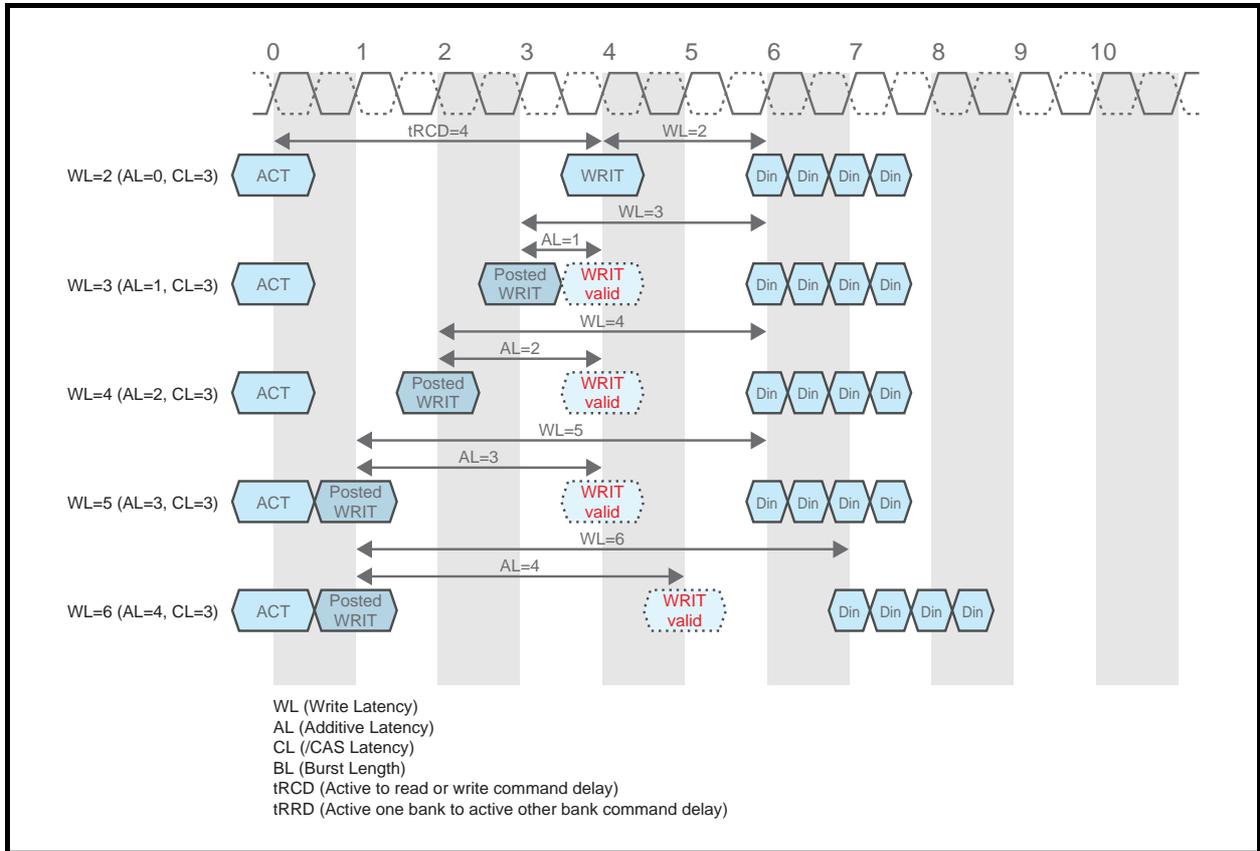


Figure 4-9 Write Latency in DDR2 SDRAM

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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